
FOREWORD

Special Section on VLSI Design and CAD Algorithms

Beyond the digitalization, the digital transformation of not only industry, such as Industry 4.0 in Germany, but also our society itself, such as Society 5.0 in Japan, is a new vision for ICT technology to change our lives and business better. In order to realize and accelerate the vision, VLSI technology and CAD algorithms have been one of the important supporting technologies for Cyber-Physical Systems (CPS), Internet of Things (IoT), artificial intelligence, and cloud systems. Hopefully this series of special sections helps researchers to acquire cutting-edge of work on VLSI design and CAD algorithms.

In this special section, we have received 20 papers. We made thorough reviews, had the paper selection meeting of all editorial committee members, and finally selected 12 papers. These papers are categorized into 5 topics: 1) Device and Circuit Modeling and Analysis, 2) Circuit Design, 3) Physical Level Design, 4) Logic Synthesis, Test and Verification and 5) High-Level Synthesis and System-Level Design. They cover a wide variety of research areas.

On behalf of the guest editorial committee, I would like to express our sincere appreciation to all authors of papers submitted to this special section. I would also like to express my thanks to all members of the guest editorial committee and all reviewers for their work on selecting papers. I should thank Prof. Shimpei Sato, Tokyo Institute of Technology and Prof. Kazuhito Ito, Saitama University for their work as Guest Editors. Thanks are also due to the IEICE headquarters for the support to this special section.

Special Section Editorial Committee Members

Guest Editors: Shimpei Sato (Tokyo Inst. of Tech.), Kazuhito Ito (Saitama Univ.)

Guest Associate Editors:

Motoki Amagasaki (Kumamoto Univ.), Makoto Ikeda (The Univ. of Tokyo), Tohru Ishihara (Nagoya Univ.), Kenichi Okada (Tokyo Inst. of Tech.), Toshiki Kanamoto (Hirosaki Univ.), Shinji Kimura (Waseda Univ.), Atsushi Kurokawa (Hirosaki Univ.), Yukihide Kohira (Univ. of Aizu), Satoshi Komatsu (Tokyo Denki Univ.), Yuichiro Shibata (Nagasaki Univ.), Kenshu Seto (Tokyo City Univ.), Tian Song (Tokushima Univ.), Kazuyoshi Takagi (Kyoto Univ.), Yasuhiro Takashima (The Univ. of Kitakyushu), Takashi Takenaka (NEC), Nozomu Togawa (Waseda Univ.), Hiroyuki Tomiyama (Ritsumeikan Univ.), Shigetoshi Nakatake (The Univ. of Kitakyushu), Yuichi Nakamura (NEC), Masanori Hashimoto (Osaka Univ.), Hiroyuki Higuchi (Fujitsu Lab.), Tetsuya Hirose (Osaka Univ.), Matthieu Parizy (Fujitsu Lab.), Takeshi Matsumoto (Ishikawa Nat'l Coll. of Tech.), Yukiya Miura (Tokyo Metropolitan Univ.), Yukio Mitsuyama (Kochi Univ. of Tech.), Shin-ichi Minato (Kyoto Univ.), Kousuke Miyaji (Shinshu Univ.), Shigeru Yamashita (Ritsumeikan Univ.), Yasushi Yuminaka (Gunma Univ.), Masaya Yoshikawa (Meijo Univ.), Hiroyuki Yotsuyanagi (Tokushima Univ.), Takayuki Watanabe (Univ. of Shizuoka)

Toshiyuki Shibuya, Guest Editor-in-Chief

Toshiyuki Shibuya (*Senior Member*) received the B.E. degree in Electrical Engineering from Waseda University, in 1985. He joined Fujitsu Laboratories Ltd., Japan, in 1985. His research interests include design and manufacturing automation, parallel processing architecture, statistical analysis and mathematical optimization. He was General Chair of the 25th Asia and South Pacific Design Automation Conference (ASP-DAC 2019).

